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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,642	08/13/2001	Andrew J. Walker	035905-0103	8019

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EXAMINER	
PERT, EVAN T	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/927,642	Applicant(s) WALKER ET AL.	
	Examiner Evan Pert	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) *13-18,21-24,27-68,70* is/are withdrawn from consideration.

5)☒ Claim(s) *25 and 26* is/are allowed.

6)☒ Claim(s) *1-12,19,20 and 69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Newly submitted claim 70 is directed to an invention that is distinct from the invention originally claimed and elected for prosecution. The species of the invention to which claim 70 is directed is a 3D non-volatile memory using "transistors" (3-terminal devices) wherein the elected species I and IV utilize "rail stacks" (i.e. two-terminal devices). Non-elected species such as Species VII specifically include "transistors." Since applicant has received an action on the merits for the originally presented and elected invention, claim 70 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12, 19-20 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (U.S. 5,835,396) in view of Wada et al. (Article entitled "Active Body-Bias SOI-CMOS Driver Circuits").

Regarding claims 1 and 69, Zhang discloses "a nonvolatile array" (i.e. 3D memory array) comprising "an array of nonvolatile memory devices" (e.g. col. 4, lines 52-54) and at least one driver circuit (i.e. "decoder" per col. 4, line 55) on a "substrate" (10).

Regarding claim 2, Zhang discloses driver circuitry as being located in "semiconductor substrate 10."

Regarding claims 19-20, Zhang discloses "EPROMS" in the array [col. 4, line 54] and that the array is a monolithic three-dimensional array of memory devices [abstract].

Zhang does not disclose the negative limitation that the "semiconductor substrate 10" is "not a bulk monocrystalline silicon substrate." However, Wada et al. teach that SOI drivers in general have "excellent speed performance over bulk ones even at large load capacitances" [conclusion] because "SOI devices operate faster and consume less power than bulk ones" [introduction].

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to use an SOI substrate (i.e. "not a bulk one") as the "semiconductor substrate 10" disclosed by Zhang for his 3D memory arrays. One of ordinary skill would have been motivated to use SOI for decoders (i.e. drivers) of Zhang because "SOI devices operate faster and consume less power" [introduction to Wada et al.] and prior art SOI driver circuits "show excellent speed performances over bulk ones" [conclusion to Wada et al.].

Regarding claims 3-12, the examiner maintains *Official Notice* that the alternative types of SOI wafers claimed were notoriously well known in the art at the time of the claimed invention

The types of SOI wafers claimed were notoriously well known at the time of filing as evidenced from applicant's lack of particular description of inventive and enabling methodology for forming the various types of SOI wafers claimed.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt *any* form of SOI substrate as the "semiconductor substrate 10" in Zhang, since all known SOI substrates provide the advantages of "faster" and "less power" for devices in general, as disclosed and taught by Wada et al. in the first sentence of the introduction.

While the Wada et al. paper specifically investigates CMOS "driver circuitry" in SOI substrates as compared to monocrystalline bulk substrates, the reference states the well known fact that SOI substrates have an advantage of speed and efficiency, for "devices" in general.

Allowable Subject Matter

3. Claims 25-26 are allowed.

4. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose the 3D array of memory devices recited by claims 25-26 corresponding to preferred methodology of manufacture as claimed in U.S. Patent 6,420,215.

Response to Arguments

5. Applicant has overcome rejections under 35 USC 112 by clarifying *the scope* of the negative limitation of "not located in a bulk monocrystalline substrate." Specifically, in the applicant's invention, there are "only three possible locations" for the driver circuit (per pages 3-4 of paper 16).

6. Applicant argues that the Wada reference is not proper for consideration in rejecting because it teaches "high speed logic circuits" rather than "memory driver circuits." However, the "decoder" circuits of Zhang are necessarily high speed logic "driver" circuits per the IEEE Authoritative Dictionary of IEEE Standards Terms, 7th Edition, p. 339, definition (4).

As set forth by the examiner in the original rejection, the decoder circuits disclosed by Zhang are necessarily "driver circuits" that send a hi or lo signals to each of the addressing lines. This is the known action of a memory decoder, to drive logic signals to the 3D memory array based on the particular address decoded by the decoders.

7. The examiner did not "combine references" as suggested by applicant, but rather presented evidence from Wada et al. that one of ordinary skill in the art would have been motivated to use an SOI substrate for "substrate 10" in Zhang. The introduction of Wada et al. states that "SOI devices operate faster and consume less power than bulk ones due to their small junction capacitances." The examiner relies on this statement for motivation in choosing the type of substrate for "substrate 10" in the invention of Zhang.

Since Zhang is silent about the type of "substrate 10" in his 3D memory invention, Wada et al. is utilized to legally show that one of ordinary skill in the art is fully aware of advantages to motivate in choosing SOI for "devices" such as "drivers."

Drivers (such as memory decoders) are clearly better if they are faster and more efficient because memory access is desirably as fast as possible (who wants to wait for memory access?) and power use is desirably as little as possible (who wants to spend more power?).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-0956.

ETP
August 11, 2003

EVAN PERT